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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,290	06/07/2001	Yoshiyuki Yanagisawa	075834.00085	9540
33448	7590	06/14/2007	EXAMINER	
ROBERT J. DEPKE			GRAYBILL, DAVID E	
LEWIS T. STEADMAN				
ROCKEY, DEPKE, LYONS AND KITZINGER, LLC			ART UNIT	
SUITE 5450 SEARS TOWER			PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/876,290

Applicant(s)

YANAGISAWA ET AL.

Examiner

David E. Graybill

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 11-15 and 20 is/are pending in the application.
- 4a) Of the above claim(s) 2-6, 12, 13 and 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 7, 11, 14 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 3-28-7, 9-13-6, 8-23-5, 12-13-4, 6-7-1 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3-28-7 has been entered.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s):

Claims 1, 11 and 14, "so as to rigidly restrict the deformation of said semiconductor modules." To further clarify, the drawings do not show the lateral position restriction mechanism or sidewalls formed or comprised so as to rigidly restrict the deformation of said semiconductor modules;

Claims 2, "two pairs of opposing side walls";

Claim 14, "two pairs of substantially parallel opposed side walls," and, "said two pairs of opposed side walls";

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if

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only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no proper antecedent basis for the claimed subject matter "side walls" and "sidewalls."

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 101 as being non-statutory because they improperly embrace or overlap two different statutory classes of invention, namely, manufacture and process of using the manufacture, which statutory classes are set forth only in the alternative in 35 U.S.C. 101. See *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990), "it is clear that appellant's independent claim 2 is intended to embrace or overlap *two* different statutory classes of invention set forth in 35 USC 101. In our view, a claim of this type is precluded by the express language of 35 USC 101"; and MPEP 2173.05(p)II.

In particular, claims 1, 11 and 14 are directed to a manufacture but the claims 1 and 11 language, "so as to rigidly restrict the deformation of said semiconductor modules," the claim 11 language, "having a single stack of the semiconductor modules therebetween," and the claims 1, 11 and 14 language, "wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module," "is removed prior to mounting the jig on a mother substrate," and, "is removed prior to mounting the jig onto a mother substrate," respectively, appears to be directed to processes of using the manufacture.

Also claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 112, second paragraph, because they are directed to both manufacture and a

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process of using the manufacture. As a result, the scope of the claims cannot be determined. See *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990), "a single claim which purports to be both a product or machine and a process is ambiguous and is properly rejected under 35 USC 112, second paragraph, for failing to particularly point out and distinctly claim the invention"; and *IPXL Holdings v. Amazon.com, Inc.*, 430 F.2d 1377, 1384, 77 USPQ2d 1140, 1145 (Fed. Cir. 2005), "it is unclear whether infringement of claim 25 occurs when one creates a system that allows the user to change the predicted transaction information or accept the displayed transaction, or whether infringement occurs when the user actually uses the input means to change transaction information or uses the input means to accept a displayed transaction. Because claim 25 recites both a system and the method for using that system, it does not apprise a person of ordinary skill in the art of its scope, and it is invalid under section 112, paragraph 2; and MPEP 2173.05(p)II.

Specifically, claims 1, 11 and 14 are directed to a manufacture but the claims 1 and 11 language, "so as to rigidly restrict the deformation of said semiconductor modules," the claim 11 language, "having a single stack of the semiconductor modules therebetween," and the claims 1, 11 and 14 language, "wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module," "is

removed prior to mounting the jig on a mother substrate," and, "is removed prior to mounting the jig onto a mother substrate," respectively, appears to be directed to processes of using the manufacture.

To further clarify, it is unclear whether infringement occurs when one creates an apparatus that is capable of being used so as to rigidly restrict the deformation of said semiconductor modules, or whether infringement occurs when the apparatus is actually used so as to rigidly restrict the deformation of said semiconductor modules; it is unclear whether infringement occurs when one creates an apparatus that is capable of being used having a single stack of the semiconductor modules therebetween, or whether infringement occurs when the apparatus is actually used having a single stack of the semiconductor modules therebetween; it is unclear whether infringement occurs when one creates an apparatus that allows the height restriction mechanism to be removed prior to mounting the jig onto a mother substrate, or whether infringement occurs when the the height restriction mechanism is actually removed prior to mounting the jig onto a mother substrate; and, it is unclear whether infringement occurs when one creates an apparatus that is capable of being used to prevent vertical displacement of an uppermost semiconductor module, or whether infringement occurs when the apparatus is actually used to prevent vertical displacement of an uppermost semiconductor module.

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The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The undescribed subject matter is the following:

Claims 1, 11 and 14, "so as to rigidly restrict the deformation of said semiconductor modules." To further clarify, the lateral position restriction mechanism or sidewalls formed or comprised so as to rigidly restrict the deformation of said semiconductor modules is not originally disclosed;

Claim 2, "two pairs of opposing side walls";

Claim 14, "two pairs of substantially parallel opposed side walls," and, "said two pairs of opposed side walls."

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following claim language:

Claims 1, 11 and 14, "the displacement," and, "the deformation."

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Normington (5397916).

At column 3, line 58 to column 10, line 47, Normington discloses the following:

Re claim 1: A multilayer semiconductor device assembly jig for minimizing the displacement (at least displacement beyond the "sides") of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process, comprising: a lateral position restriction mechanism "sides"/131, 132 being used for positioning and aligning a plurality of

stacked semiconductor modules "subassemblies" on a solid base member 81/223 with their respective lateral positions mutually restricted, the lateral position restriction mechanism formed at a width slightly more than but substantially equal to a width of a rigid portion 21, 23, 24 "the lead and polyimide layer provides adequate stiffness along the edge of the die" of said plurality of semiconductor modules so as to be capable of being used to rigidly restrict the deformation of said semiconductor modules; a removable height restriction mechanism 91/252 disposed opposite said base member and which interfaces with said lateral position restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member and which is inherently capable of being removed prior to mounting the jig onto a mother substrate "printed circuit board"; a mother substrate alignment mechanism 92/253 inherently capable of being used for providing alignment with reference to the mother substrate on which the jig will be mounted; and further wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips 21 secured to a printed wiring board 51 that has electrical connections 24 on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections "solder glass" and "Die 203 is attached to separator 201 by conductive epoxy, eutectic bonding, solder or glass" between respective top and bottom surfaces thereof.

Re claim 2: The multilayer semiconductor device assembly jig according to claim 1, wherein said lateral position restriction mechanism comprises a substantially rectangular-shaped member formed from two pairs of opposing side walls 131, 132 and which is positioned on said base member and which has a storage space for storing said semiconductor modules in a layered state, wherein an inner wall surface of said storage space constitutes said lateral position restriction mechanism.

Re claim 7: The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism comprises: a cover member secured over or on said semiconductor module lateral position restriction mechanism.

Re claim 11: A multilayer semiconductor device assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process, comprising; a lateral position restriction mechanism for positioning and aligning a plurality of stacked semiconductor modules on a solid base member with their respective lateral positions mutually restricted, the lateral position restriction mechanism comprised of two opposed side walls having a single stack of the semiconductor modules therebetween, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to be

inherently capable of being used to rigidly restrict the deformation of said semiconductor modules; a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member, wherein said height restriction mechanism is inherently capable of being removed prior to mounting the jig on a mother substrate; a mother substrate alignment mechanism inherently capable of being used for providing alignment with reference to the mother substrate on which the jig will be mounted; and further wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips secured to a wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 14: An assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process comprising: two pairs of substantially parallel opposed side walls formed on a solid base member, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to be inherently capable of being used rigidly restrict the deformation of said

semiconductor modules; a removable cover member located opposite said base member and which interfaces with the side walls; an internal void defined by said two pairs of opposed side walls providing a reception area for a plurality of semiconductor modules such that, when disposed within the void, the modules are aligned and their lateral motion (at least their lateral motion beyond the side walls) is prevented by the side walls, and wherein the semiconductor modules are comprised of at least one chip and one wiring board; and further wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module.

Re claim 20: The multilayer semiconductor device assembly jig according to claim 1, wherein said mother substrate alignment mechanism is formed in said lateral position restriction mechanism.

In any case, the following language is statements of intended use of the claimed apparatus:

Re claim 1: "A multilayer semiconductor device assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process"; "a lateral position restriction mechanism for positioning and aligning a plurality of stacked semiconductor modules on a solid base member with their respective lateral positions mutually restricted"; a width of a rigid portion of

said plurality of semiconductor modules so as to rigidly restrict the deformation of said semiconductor modules; a removable height restriction mechanism"; "for restricting an entire height of said semiconductor modules layered on said base member and which is removed prior to mounting the jig onto a mother substrate; a mother substrate alignment mechanism for providing alignment with reference to the mother substrate on which the jig will be mounted; "wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections."

Re claim 2: "a storage space for storing said semiconductor modules in a layered state, wherein an inner wall surface of said storage space constitutes said lateral position restriction mechanism."

Re claim 11: "A multilayer semiconductor device assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process"; "a lateral position restriction mechanism for positioning and aligning a plurality of stacked semiconductor modules on a solid base member with their respective lateral positions mutually restricted"; "having a single stack of the semiconductor modules therebetween"; "a width of a rigid portion of said

plurality of semiconductor modules so as to rigidly restrict the deformation of said semiconductor modules; a removable height restriction mechanism"; "for restricting an entire height of said semiconductor modules layered on said base member, wherein said height restriction mechanism is removed prior to mounting the jig on a mother substrate; a mother substrate alignment mechanism for providing alignment with reference to the mother substrate on which the jig will be mounted; "wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips secured to a wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof."

Re claim 14: An assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process"; "a width of a rigid portion of said plurality of semiconductor modules so as to be inherently capable of being used rigidly restrict the deformation of said semiconductor modules; a removable cover member"; "a reception area for a plurality of semiconductor modules such that, when disposed within the void, the modules are aligned and their lateral motion is prevented by the side walls, and wherein the semiconductor modules are comprised of at least one chip and one wiring board"; "the

removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module."

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed apparatus and the apparatus of Normington. Further, because the apparatus of Normington appears to have the same structure as the claimed apparatus, it appears to be capable of being used for the intended uses, and the statements of intended use do not patentably distinguish the claimed apparatus from the apparatus of Normington. The manner in which a product operates is not germane to the issue of patentability of the product; *Ex parte Wikdahl* 10 USPQ 2d 1546, 1548 (BPAI 1989); *Ex parte McCullough* 7 USPQ 2d 1889, 1891 (BPAI 1988); *In re Finsterwalder* 168 USPQ 530 (CCPA 1971); *In re Casey* 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; *Ex parte Thibault*, 164 USPQ 666, 667 (Bd. App. 1969). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. *In re Danley*, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

It is especially noted that, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). Therefore, all of the language directed to the semiconductor modules, including "printed circuit board" and "a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules so as to rigidly restrict the deformation of said semiconductor modules" does not impart patentability to the claims.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the alternative, claims 1, 2, 7, 11, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Normington (5397916).

Normington is applied as it is applied to claims 1, 2, 7, 11, 14 and 20 *supra*.

However, Normington does not appear to disclose verbatim the particular claimed width.

Notwithstanding, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular dimension because applicant has not disclosed that, in view of the applied prior art, the dimension is for a particular **unobvious** purpose, produces an unexpected result, or is otherwise critical, and it appears *prima facie* that the apparatus would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777

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(Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Applicant's amendment and remarks filed 3-28-7 have been fully considered and are treated *supra* and *infra*.

Applicant argues, "Regarding the Examiner's objection to the drawings under 37 C.F.R. 1.83(a), Applicants submit that the feature claimed in claims 2 and 14 (two pairs of opposing side walls forming a rectangular shape) is clearly shown in the drawings and described in the specification. Figures 2(d), 2(e), 3, and 4, while being limited to a cross-section view of the box-shaped member, when read in light of the specification (see page 15), clearly teaches that the semiconductor modules 2 are surrounded on all sides by the walls of the body 15 in these embodiments. This necessarily requires the box-shaped member be comprised of two pair of parallel opposed side walls of the body 15."

This argument is respectfully traversed because Figures 2(d), 2(e), 3, and 4, when read in light of the specification at page 15 do not disclose that the semiconductor modules 2 are surrounded on all sides by the walls of the body 15 in these embodiments.

Relatedly, applicant contends, "the plan view of Fig. 5 (b), while illustrating the use of pins 32 instead of side-walls of the body 15, shows the

pins/lateral position restriction mechanism is arranged in a rectangular 'box-shape' comprised of two pairs of parallel opposing side walls."

This contention is respectfully deemed unpersuasive and traversed because Fig. 5(b) is directed to a non-elected species that is not disclosed as usable together with the mutually exclusive species of Fig. 4. Moreover, Fig. 5(b) does not show "pins/lateral position restriction mechanism is arranged in a rectangular 'box-shape' comprised of two pairs of parallel opposing side walls." Specifically, the pins/lateral position restriction mechanism 32 are not comprised of two pairs of parallel opposing side walls.

In addition, applicant asserts, "Applicants have amended the claim to more specifically require that the lateral restriction mechanism be formed in a rectangular shape comprised of two pairs of opposing side-walls. As discussed above, this structure is clearly supported by Figures 2(d), 2(e), 3, and 4 and page 15 of the specification. . . . In regard to the Examiner's rejection of claims 2, 7, 11, 14, and 16 - 18 under 35 U.S.C. §112, second paragraph, as being indefinite for alternately using the terms 'box-shaped' or 'two pairs of opposing side walls,' Applicants submit that there is more than adequate support for these terms in the specification and drawings. As discussed above, Figures 2(d), 2(e), 3, and 4, while being limited to a cross-section view of the box-shaped member, when read in light of the specification (see page 15), clearly teaches that the semiconductor modules

2 are surrounded on all sides by the walls of the body 15 in these embodiments."

These assertions are respectfully deemed unpersuasive and traversed because applicant merely cites the specification without elucidation, and the citations do not support the assertions, and, as elucidated in the rejections, Figures 2(d), 2(e), 3, and 4 and page 15 of the specification do not disclose the claim limitations, "two pairs of opposing side walls," "two pairs of substantially parallel opposed side walls," and, "said two pairs of opposed side walls."

Applicant also alleges, "However, such a structure fails to anticipate the currently claimed invention for at least the reason that by not rigidly interfacing the semiconductor dies 61 - 64 with the sidewall 70 of the subassembly, the Normington reference would fail to prevent the deformation of the semiconductor dies during a subsequent manufacturing process such as reflow . . . By not forming the sides of the sub-assembly to slightly more than but substantially equal to the width of the ridge portion of the dies, the Normington reference falls to prevent the deformation of the dies during a subsequent manufacturing process.

These allegations are respectfully deemed unpersuasive because the scope of the claims is not limited to a subsequent manufacturing process such as reflow and Normington is not necessarily applied to the rejections

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for this disclosure. In any case, these allegations are unsupported by proof or a showing of facts; hence, they essentially amount to mere conjecture and they are of no probative value. See MPEP 716.01(c), and, Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989) (statement in publication dismissing the "preliminary identification of a human b - NGF - like molecule" in the prior art, even if considered to be an expert opinion, was inadequate to overcome the rejection based on that prior art because there was no factual evidence supporting the statement); In re Beattie, 974 F.2d 1309, 24 USPQ2d 1040 (Fed. Cir. 1992) (declarations of seven persons skilled in the art offering opinion evidence praising the merits of the claimed invention were found to have little value because of a lack of factual support); Ex parte George, 21 USPQ2d 1058 (Bd. Pat. App. & Inter. 1991) (conclusory statements that results were "unexpected," unsupported by objective factual evidence, were considered but were not found to be of substantial evidentiary value).

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR:

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours:

Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (571) 273-8300.



David E. Graybill
Primary Examiner
Art Unit 2822

D.G.

5-Jun-07